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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/662,725	09/15/2003	Melissa Ann Diercks	138681	1504

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EXAMINER	
KRAMSKAYA, MARINA	
ART UNIT	**PAPER NUMBER**
2858	

DATE MAILED: 06/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/662,725	DIERCKS ET AL.	
	Examiner	Art Unit	
	Marina Kramskaya	2858	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *10 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-2, 6-11, 13-14, & 18-23 are rejected under 35 U.S.C. 102(b) as being anticipated by Weeks, US 5,168,261.

As per Claims 1 & 13, Weeks discloses a method and arrangement for testing an electrical switchgear system (ABS.), comprising:

applying an analog signal (from **18**) to a node (**14**) in said electrical switchgear system, wherein said node monitors a power line signal (i.e. during operation monitors **9**, during test monitors **18**) and controls a breaker **6** based on said power line signal, and wherein said analog signal simulates said power line signal (i.e. simulates electrical operation, column 1, line 12); and

receiving data representing a status of said breaker (through interface **8**).

As per Claims 2 & 14, Weeks further discloses the method and arrangement for testing an electrical switchgear system, wherein the data is received (by **8**) from at least one of said node **14** or said breaker **6**.

As per Claims 6 & 18, Weeks further discloses the method and arrangement for testing an electrical switchgear system, wherein the application of the signal (from 18) is performed while said node **14** monitors said power line signal (column 3, lines 37-40).

As per Claims 7 & 19, Weeks further discloses the method and arrangement for testing an electrical switchgear system, wherein said analog signal simulates a fault condition of said power line signal (column 5, lines 32-35).

As per Claims 8 & 20, Weeks further discloses the method and arrangement for testing an electrical switchgear system, wherein said analog signal simulates a non-fault (i.e. "normal" operation) condition of said power line signal. (column 3, lines 46-48).

As per Claims 9 & 21, Weeks further discloses the method and arrangement for testing an electrical switchgear system, wherein additional modifying of said analog signal based on said status of said breaker is provided; and additional data representing said status of said breaker is received (column 3, lines 56-59). In the instant case, the operator modifies the signal of the signal, and the node continues to receive data regarding the status of the breaker.

As per Claims 10 & 22, Weeks further discloses the method and arrangement for testing an electrical switchgear system,

wherein said analog signal is a first analog signal (i.e. continuous signal from **18**), said node is a first node (**14**: "circuit breaker control #1"), said breaker is a first breaker (**6**: "circuit breaker #1"), and said power line signal is a first power line signal,

wherein said method further comprises applying, a second analog signal (i.e. continuous signal from **18**, plugged into second receptacle **24**) to a second node (**14**: "circuit breaker control #1") in said electrical switchgear system,

wherein said second node (**14**: "circuit breaker control #2") monitors a second power line signal and controls a second breaker (**6**: "circuit breaker #2") based on said second power line signal, and

wherein said second analog signal simulates said second power line signal (i.e. simulates electrical operation, column 1, line 12).

Weeks does not explicitly teach applying the second signal simultaneously with the application of the first analog signal.

However, it would have been obvious to a person of ordinary skill in the art to apply the second signal simultaneously with the application of the first analog signal, since an additional test receptacle (**24**) is provided for the second node. The benefit of applying the two test signals simultaneously would be to reduce testing time for the switchgear system.

As per Claims 11 & 23, Weeks further discloses the method and arrangement for testing an electrical switchgear system, further comprising measuring a time required for the said breaker to trip based on timestamps of said data (column 5, lines 16-18). Although, Weeks does not explicitly teach measuring the predetermined amount of time, it is inherent for the system to measure the said predetermined time, for the tester to function.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 3-5, 12, 15-17, & 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Weeks, in view of Baker, US 5,737,168.

As per Claims 3-5 & 15-17, Weeks discloses a method and arrangement for testing an electrical switchgear system, as applied to claims 1 & 13, above.

Weeks does not explicitly disclose a method and arrangement for testing an electrical switchgear system, wherein

the analog signal has a magnitude of less than about 10 volts peak-to-peak (column 11, lines 58-59);

the analog signal has a magnitude of about 2.5 volts peak-to-peak (column 11, lines 58-59);

the analog signal has a magnitude of less than or equal to about 10% of a magnitude of said power line signal (column 11, lines 58-59, the test signal is about 2%).

Therefore, it would have been obvious to a person of ordinary skill in the art to have the test analog signal be less than about 10 volts peak-to-peak less, in particular about 2.5 volts peak-to-peak, and less than or equal to about 10% of a magnitude of the power line signal, in order to avoid damage to the circuit which could be caused be the high power line voltage.

As per Claims 12 & 24, Weeks discloses a method and arrangement for testing an electrical switchgear system (ABS.), comprising:

applying a first analog signal (continuous signal from **18**) to a first node (**14**: "circuit breaker control #1") in said electrical switchgear system, wherein said first node monitors a first power line signal and controls a first breaker (**6**: "circuit breaker #1") based on said first power line signal, and wherein said first analog signal simulates said first power line signal (i.e. simulates electrical operation, column 1, line 12);

applying a second analog signal (continuous signal from **18**, plugged into second receptacle **24**) to a second node (**14**: "circuit breaker control #2") in said electrical

switchgear system, wherein said second node monitors a second power line signal and controls a second breaker (**6**: "circuit breaker #2") based on said second power line signal, and wherein said second analog signal simulates said second power line signal (i.e. simulates electrical operation, column 1, line 12); and

receiving data (by **8**) from said first node representing a status of said first breaker.

Weeks does not explicitly teach applying the second signal simultaneously with the application of the first analog signal, and Weeks does not disclose the first analog signal having a magnitude of less than or equal to about 10% of a magnitude of the first power line signal.

Baker discloses first analog signal having a magnitude of less than or equal to about 10% of a magnitude of the first power line signal (column 11, lines 58-59, the test signal is about 2%).

However, it would have been obvious to a person of ordinary skill in the art to apply the second signal simultaneously with the application of the first analog signal, since an additional test receptacle (**24**) is provided for the second node. The benefit of applying the two test signals simultaneously would be to reduce testing time for the switchgear system. Further, it would have been obvious to a person of ordinary skill in the art to have the test analog signal be less than or equal to about 10% of a magnitude of the first power line signal, in order to avoid damage to the circuit which could be caused be the high power line voltage.

5. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Weeks, in view of Lavoie et al., US 6,798,209.

Weeks discloses a method comprising instruction for a operator for testing an electrical switchgear system, the instructions comprising:

apply an analog signal (from **18**) to a node (**14**) in said electrical switchgear system, wherein said node monitors a power line signal (i.e. during operation monitors **9**, during test monitors **18**) and controls a breaker (**6**) based on said power line signal, and wherein said analog signal simulates said power line signal (i.e. simulates electrical operation, column 1, line 12); and

receive data representing a status of said breaker (by interface **8**).

Weeks does not disclose storage medium comprising instructions for controlling a processor for testing an electrical switchgear system.

Lavoie discloses storage medium **123** comprising instructions for controlling a processor (in **123**) for testing an electrical switchgear system.

Therefore, it would have been obvious to a person of ordinary skill in the art to include a storage means and a processor, as taught by Lavoie, in the testing system of Weeks, in order to replace the human operator with a processor, which would reduce operator error.

6. Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Weeks, in view of Baker and Lavoie.

Weeks discloses Weeks discloses a method comprising instruction for a operator for testing an electrical switchgear system, the instructions comprising:

applying a first analog signal (continuous signal from **18**) to a first node (**14**: "circuit breaker control #1") in said electrical switchgear system, wherein said first node monitors a first power line signal and controls a first breaker (**6**: "circuit breaker #1") based on said first power line signal, and wherein said first analog signal simulates said first power line signal (i.e. simulates electrical operation, column 1, line 12);

applying a second analog signal (continuous signal from **18**, plugged into second receptacle **24**) to a second node (**14**: "circuit breaker control #2") in said electrical switchgear system, wherein said second node monitors a second power line signal and controls a second breaker (**6**: "circuit breaker #2") based on said second power line signal, and wherein said second analog signal simulates said second power line signal (i.e. simulates electrical operation, column 1, line 12); and

receiving data (by **8**) from said first node representing a status of said first breaker.

Weeks does not explicitly teach applying the second signal simultaneously with the application of the first analog signal, and Weeks does not disclose the first analog signal having a magnitude of less than or equal to about 10% of a magnitude of the first power line signal. Weeks does not disclose storage medium comprising instructions for controlling a processor for testing an electrical switchgear system.

Baker discloses first analog signal having a magnitude of less than or equal to about 10% of a magnitude of the first power line signal (column 11, lines 58-59, the test signal is about 2%).

Lavoie discloses storage medium **123** comprising instructions for controlling a processor (in **123**) for testing an electrical switchgear system.

However, it would have been obvious to a person of ordinary skill in the art to apply the second signal simultaneously with the application of the first analog signal, since an additional test receptacle (**24**) is provided for the second node. The benefit of applying the two test signals simultaneously would be to reduce testing time for the switchgear system. Further, it would have been obvious to a person of ordinary skill in the art to have the test analog signal be less than or equal to about 10% of a magnitude of the first power line signal, in order to avoid damage to the circuit which could be caused be the high power line voltage. Yet further, it would have been obvious to a person of ordinary skill in the art to include a storage means and a processor, as taught by Lavoie, in the testing system of Weeks, in order to replace the human operator with a processor, which would reduce operator error.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Tiemann et al., US 6,472,882, discloses a test for a switchgear system with a simulated power line signal.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Marina Kramskaya whose telephone number is (571)272-2146. The examiner can normally be reached on M-F 7:00-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edward Lefkowitz can be reached on (571)272-2180. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Marina Kramskaya
Examiner
Art Unit 2858

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5/31/2005

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